Engineering 73 Report
Charge Storage Diode Transient Behaviors

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Acknowledgements This document is a brief summary of a large quantity of material on p-n junction charge storage diodes contained in the references. The presentation of material therefore closely follows that of the sources, however in a (hopefully) appropriately abbreviated manner.

1 Abstract

The charge storage diode is a special p-n or p-i-n junction diode that finds application in high frequency multiplier circuits, comb generators, and pulse generators. The diodes are also known as *step recovery* or *snap off* diodes, due to the sharp transitions that can be achieved with them. This report documents the transient behavior of these devices, explores various modeling techniques, and pursues applicability of such diodes to pulse generator circuits.

2 Charge Control Analysis

One way to quantify the action of a p-n junction diode is to account for the charge at the junction. Since the silicon device operation is governed by the action of the minority carriers, we define Q as the excess minority carrier charge in a given volume of semiconductor material. The volume specified with Q is not that of the entire semiconductor, in which case the total concentration would necessarily be zero. Thus, we can write the law of charge conservation as

$$\frac{dQ}{dt} + \frac{Q}{\tau} = i$$

The rate of recombination of carriers within the semiconductor volume increases with the number of carriers, accounting for the $\frac{1}{\tau}Q$ factor in the charge conservation equation. We impose the initial condition of some charge injection into our volume at $t = 0$ of value Q_0. However, another mechanism by which charge is introduced into the volume is by a current flowing across it, and if the current is assumed to flow *into* the volume, then we have the i term in the conservation equation. i represents those carriers in the current that become excess minority carriers once inside the volume.

3 Storage and Transition Times

Every standard p-n junction diode exhibits transient behavior when the applied voltage changes before reaching steady state carrier concentrations. In the reverse bias condition, very little current flows across the p-n junction because only the minority carriers on opposite sides of the junction have the charge of the proper sign for conduction. The minority carrier distribution under reverse bias is shown in Figure 1. Since the excess minority carriers are heavily depleted from the space

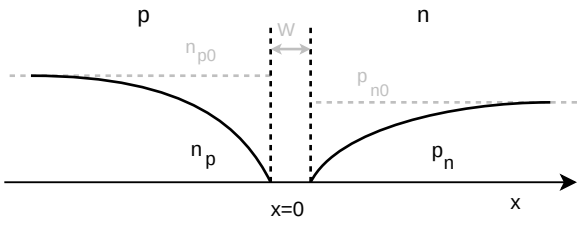

Figure 1: Reverse Bias Excess Minority Carrier Concentration

charge region, the width of the region grows, as expressed in the equation for W below.

$$W = \left\{ \frac{2\epsilon_s(V_{bi} + V_R)}{q} \left[\frac{N_A + N_D}{N_A N_D} \right] \right\}^{1/2}$$

In the forward bias condition, the space charge region width W decreases and the steady state density of minority charge carriers is large, since there is a ready supply of them from the other side of the junction where they are majority carriers. The forward bias minority carrier distribution is shown in Figure 2.

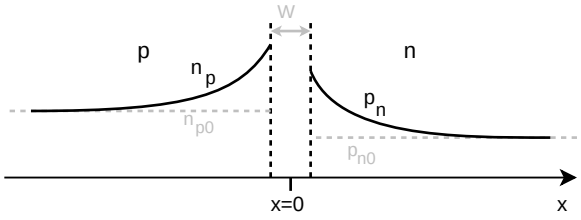

Figure 2: Forward Bias Excess Minority Carrier Concentration

When the external applied voltage suddenly switches from a forward to a reverse bias, the diode current cannot immediately achieve its steady state value of essentially zero current flow. The diode will continue to conduct until the excess minority carriers are eliminated from the space charge region and regain their original reverse bias distribution (Figure 1). A simple circuit illustrating this operation is given in Figure 3.

Upon switching to an external reverse bias, the excess minority carrier concentration gradients at the p-n junction cannot be maintained, and the gradients decrease. The *storage time* t_s is the time required for the distributions to reach their thermal equilibrium levels. During this time, there

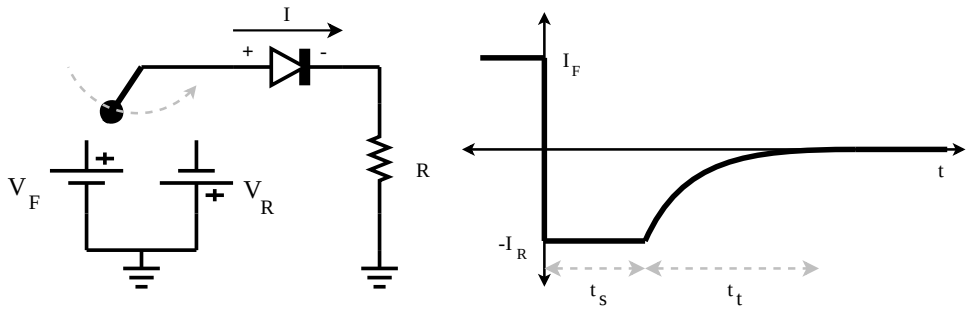

Figure 3: Example Circuit for Observing Diode Transient Behavior

are still adequate numbers of carriers in the space charge region to sustain a current flow, and hence the diode current remains at a relatively constant negative value. After the carriers are depleted, the diode enters the transition region, in which the voltage starts to change. The remainder of excess carriers are removed, and the concentrations drop below the thermal equilibrium values, resulting in an increased space charge region width as the reverse voltage condition reaches steady state. Another way to account for the transition region is to consider it as the time required to charge the built-in reverse bias junction capacitance that results due to the separation of charges in the depleted state.

The total turn-off or reverse-recovery time for the diode is thus the sum of these two effects.

$$t_{rr} = t_s + t_t$$

The storage time can be determined using charge control analysis. First, a sufficient forward bias is applied so that the forward diode current I_F can develop an excess charge in the junction volume of $Q_0 = \tau I_F$. Then, at $t = 0$, the current is immediately switched to $-I_R$. Solving the charge conservation equation with the condition $Q = Q_0|_{t=0}$ and denoting the storage time as the time when the excess charge is depleted from the volume $Q = 0|_{t=t_s}$. The solution is given as

$$t_s = \tau \ln\left(1 + \frac{I_F}{I_R}\right)$$

To calculate the transition time, an approximate worst case situation is chosen in which the transition capacitance C_T is assumed always to be at its maximal value. Then, the charge-up time can be conservatively approximated as $4RC_T$.

4 Device Operation

In a charge storage diode, majority carriers that are moved across the junction by an external forward bias also create some minority carriers in both regions [3]. The minority carrier lifetime is designed to be long enough that these carriers do not immediately recombine, and hence some steady state excess charge is stored at the junction. When a reverse bias is applied, the carriers in the junction are removed and return to the appropriate sides of the diode. Thus, current continues to flow until the charges have been removed, at which point the diode presents an extremely high

impedance and current flow abruptly halts. If the reverse bias junction capacitance is small enough, the transition times less than 100 ps can be achieved.

This mechanism is is achieved by controlling the doping so that the doping level gradually decreases as the junction is approached from either side. This way, the minority carriers are relatively restricted to a narrow region around the junction, and are thus prevented from diffusing to far away from the junction before the reverse bias is applied. The other requirement is that the minority carriers must not recombine too quickly before the reverse bias forces them out of the space charge region, otherwise the transition sharpness will be greatly reduced. The thermal equilibrium carrier concentrations that result from the doping are shown in Figure 4. It can be seen that the doping gradient forces the excess carriers to build up close to the junction, and also that once they are depleted, the carrier concentration is indeed very low, resulting in a sharp transition to the high impedance state. In fact, the withdrawal of the excess minority carriers from the space charge region directly charges the transition capacitance as the carriers are drawn back to the sides where they become once again majority carriers. Thus, the transition time is very short once the junction is depleted. Furthermore, the reduced doping near the junction increases the distance between the charges that create the junction capacitance, and thus the charge storage diode capacitances tend to be quite small.

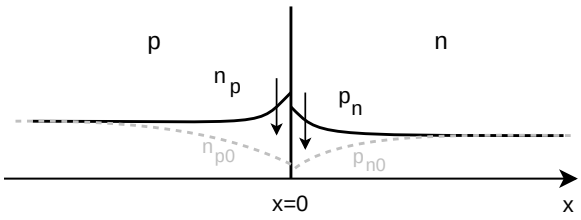

Figure 4: Charge Storage Diode Minority Carriers Under Forward Bias

To successfully use the snap action of a charge storage diode in pulse generator circuits, some consideration must be given to the input voltage that creates the reverse bias condition. If the input voltage transition is not fast enough, the stored junction charge will have enough time to achieve the appropriate carrier distribution for the amount of steady state current flowing at each moment. At the point that input voltage is 0, the stored charge will also be depleted to equilibrium levels, and thus the input voltage cannot go much lower before all of the stored charge is completely eliminated, reducing considerably the step amplitude. Thus the input voltage must be fast enough to sufficiently reverse bias the diode junction before the storage phase is completed.

5 Device Modeling

Modeling the charge storage diode with standard circuit simulation tools is complicated by the fact that SPICE does not include the transition time as a parameter in the basic diode model. One way to simulate a circuit based on a charge storage diode is to construct an idealized subcircuit that simulates the forward bias voltage drop, package parasitics, and contains an ideal switch to provide instant transitions. Such equivalent circuit models are proposed by [3], and are included below.

- C_p = package capacitance

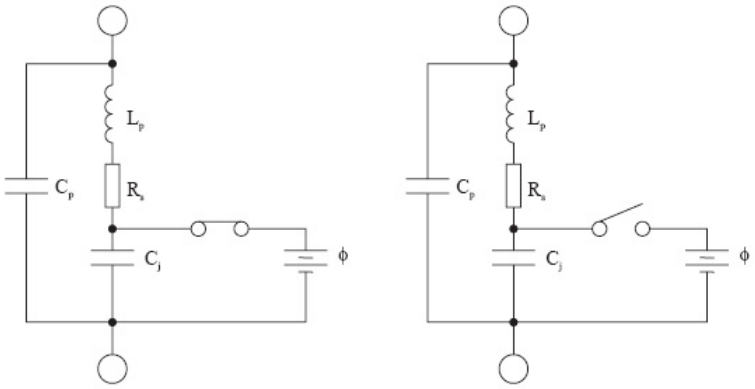

Figure 5: Equivalent Circuit Models for Forward and Reverse Bias ([3])

- L_p = package inductance
- R_s = dynamic series resistance
- C_j = reverse bias junction capacitance
- ϕ = built-in potential (~ 0.7 V)

A less idealized modeling approach is taken by modifying the available SPICE parameters to most closely mimic the charge storage diode operation. Model parameters are available from Aeroflex/Metelics for their series of silicon step recovery diodes. The critical parameters determining the charge storage behavior of the diode are `TT` (transit time) and `CJO` (junction capacitance).The parameters for the MMD-805 device are given below.

```
.MODEL DMMD805 (IS=500.0E-15 N=1.3 RS=0.13 CJ0=4.55e-9 VJ=0.5
M=0.235 XTI=3.0 EG=1.12 BV=60 IBV=10E-6 TT=30E-9)
```

A simple circuit to test the SPICE model of the charge storage diode is given in Figure 6.

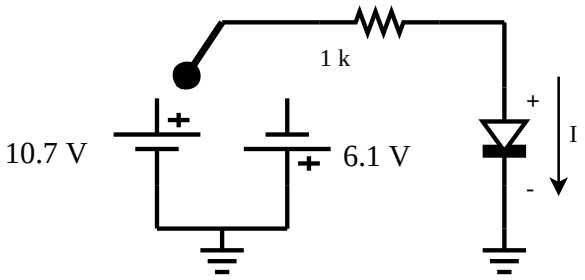

Figure 6: Charge Storage Diode SPICE Test Circuit ([9])

The SPICE netlist is given below. Three different values of reverse bias junction capacitance C_{J0} are used to illustrate the effect of the capacitance on the step recovery time. It is clear that this capacitance along with the dynamic series resistance R_s defines the transition time of the diode, as expected from the preceding charge control analysis.

```
* example srd simulation with various capacitances
V1 1 0 pulse(10.7 -6.1 5e-9 0 0 1us 10us)

R1 1 2 1k
D1 2 3 DMMD805c1
Vm1 3 0 DC 0

R2 1 5 1k
D2 5 6 DMMD805c2
Vm2 6 0 DC 0

R3 1 8 1k
D3 8 9 DMMD805c3
Vm3 9 0 DC 0

.model DMMD805c1 D(Is=500e-15 N=1.3 Rs=.13 CJO=3.3e-12
Vj=0.5 M=0.235 XTI=3.0 EG=1.12 IVB=10e-6 TT=10e-9 Bv=60 Ibv=0.1p)
.model DMMD805c2 D(Is=500e-15 N=1.3 Rs=.13 CJO=2.3e-12
Vj=0.5 M=0.235 XTI=3.0 EG=1.12 IVB=10e-6 TT=10e-9 Bv=60 Ibv=0.1p)
.model DMMD805c3 D(Is=500e-15 N=1.3 Rs=.13 CJO=1.3e-12
Vj=0.5 M=0.235 XTI=3.0 EG=1.12 IVB=10e-6 TT=10e-9 Bv=60 Ibv=0.1p)

.control
tran .05ns 35ns
plot i(Vm1) i(Vm2) i(Vm3)
.endc
.end
```

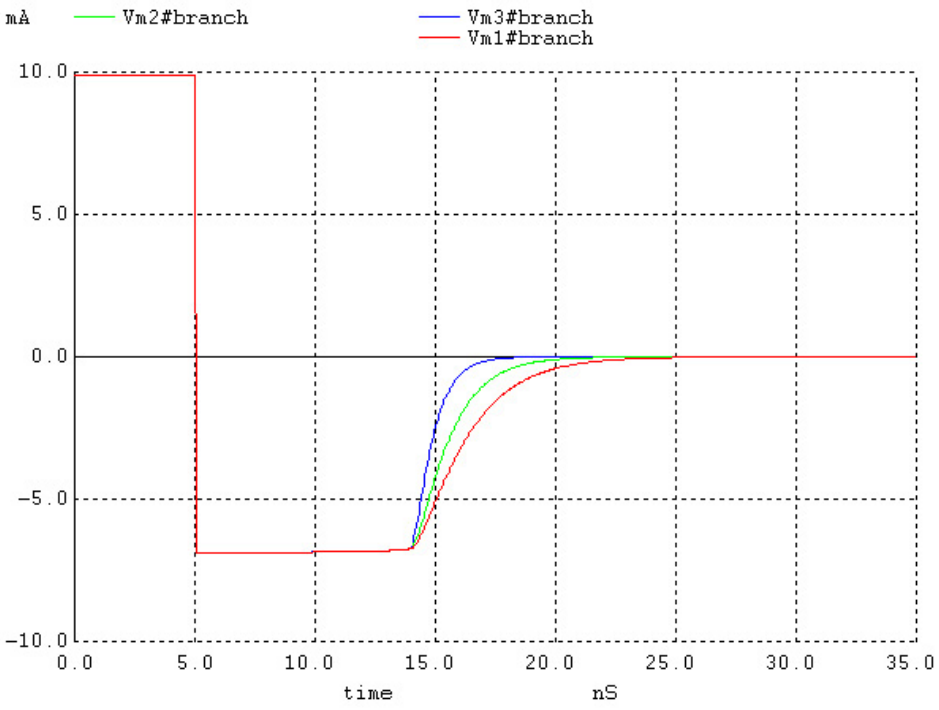

Figure 7: SPICE Simulation Result

The SPICE simulation results clearly show the correct operation of the charge storage diode.

After reverse bias is applied by the input voltage, the diode continues to conduct relatively constantly for the storage period, after which a highly nonlinear transition to the high impedance state takes place. The storage time remains effectively constant regardless of the junction capacitance, as it dependent primarily on the ratio of the forward current to the reverse bias current. Note that this simulation only demonstrates the charge storage mechanism given an ideal current step.

6 Pulse Generator

A simple charge storage diode based pulse generator circuit is shown in Figure 8.

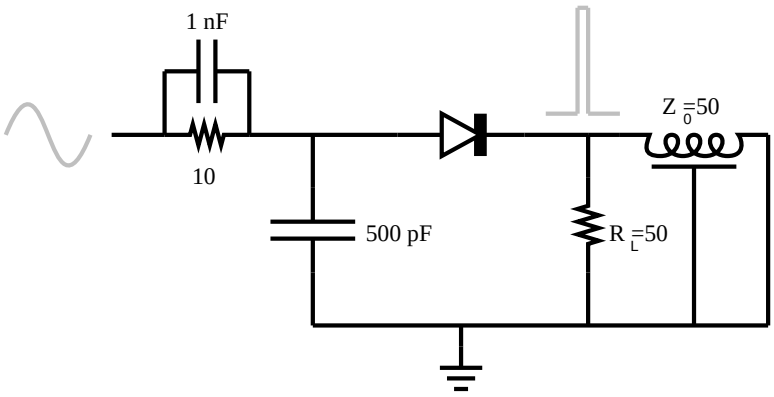

Figure 8: Pulse Generator Circuit

When the input sinsoidal voltage is positive, the diode conducts and accumulates charge in the junction. As expected, when the voltage changes polarity, the diode continues to conduct for the storage period, after which a sharp transition in the diode current produces a rapid change in the voltage across the load resistance. Initially, the cathode of the diode sees a voltage division between the load and the characteristic impedance of the delay line. The delay line is shorted, so the voltage must go to zero at the end of it, pulling down the voltage on the load resistance to ground after a time equal to the round-trip propagation delay in the line. This results in the very narrow high amplitude voltage pulse seen on the load. The SPICE netlist and simulation result are included below.

```
* example pulse generator simulation

Vin 1 0 sin(0 5 10e6 0 0)
C1 1 2 1nF
R1 1 2 10
C2 2 0 500pF
Vm 2 3 DC 0
D1 3 4 DMMD805c3
Rl 4 0 50
T1 4 0 0 0 ZO=50 TD=200pS

.model DMMD805c3 D(Is=500e-15 N=1.3 Rs=.13 CJO=1.3e-12
Vj=0.5 M=0.235 XTI=3.0 EG=1.12 IVB=10e-6 TT=10e-9 Bv=60 Ibv=0.1p)

.control
tran .05ns 100ns
```

```
plot V(1) V(4) i(Vm)*10
.endc
.end
```

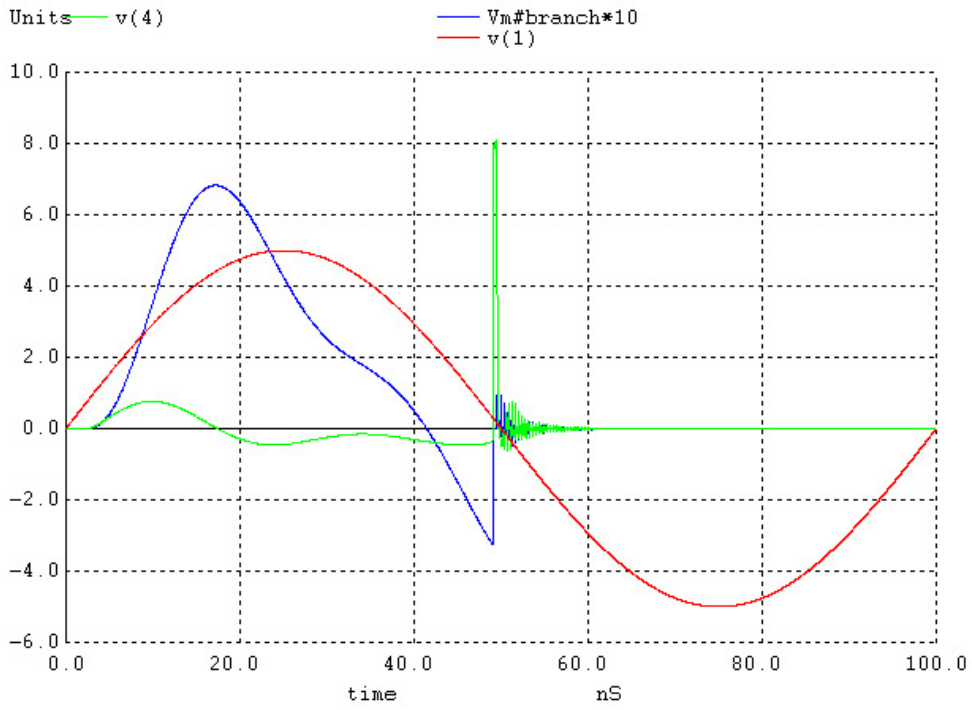

Figure 9: Pulse Generator SPICE Simulation Result

The blue curve shows the diode current. The time when the diode conducts a negative current is exactly the storage time, after which the transition to high impedance results in the snap action. The DC current that was previously flowing through the delay line now is cut off, and the energy stored in the line has nowhere to go but through the matched 50 Ω load impedance. This current reversal results in the voltage spike across R_L, whose width is dictated by the amount of energy storage in the delay line, and hence the length of the line.

7 Conclusions

The charge storage diode is indeed a useful device for generating very sharp pulse waveforms. The mechanism of its operation can be explained in a straightforward manner through charge conservation analysis, and by considering the doping techniques used to specialize the diode's operation. To aid the high frequency circuit designer with modeling, the proper choice of SPICE simulation parameters was shown to provide at least a 1^{st} order approximation of the charge storage operation of the diode.

References

[1] Chudobiak, Michael J. "*New Approaches for Designing High Voltage, High Current Silicon Step Recovery Diodes for Pulse Sharpening Applications.*" 1996. Avtech Electrosystems. 24 Apr. 2006 <http://www.avtechpulse.com/papers/thesis/>.

[2] Dobos, Aron. "*Engineering 90 Draft Report: High Speed Time Domain Reflectometer.*" Apr. 2006. Swarthmore College Engineering. 24 Apr. 2006 <http://www.engin.swarthmore.edu/∼adobos1/e90/e90draft.pdf>

[3] Kirkby, David. "*Chapter 5: Pulse Generators.*" Apr. 1999. UCL Dept. of Medical Physics and Bioengineering. 24 Apr. 2006 <http://www.medphys.ucl.ac.uk/research/borl/homepages/davek/phd/chapter5.pdf>.

[4] Li, Sheng S. "*Chapter 11: P-N Junction Diodes.*" 20 Oct. 2005. 24 Apr. 2006 <http://www.sli.ece.ufl.edu/eel6383/Chapter11.pdf>.

[5] Millman, Jacob, and Herbert Taub. *Pulse, Digital, and Switching Waveforms.* New York: McGraw-Hill Book Company, 1965.

[6] Milnes, Arthur G. *Semiconductor Devices and Integrated Electronics.* New York: Van Nostrand Reinhold Company, 1980.

[7] Neaman, Donald A. *Semiconductor Physics and Devices.* 3rd ed. New York: McGraw Hill, 2003.

[8] "*Spice Models for Metelics Step Recovery Diodes.*" 11 Mar. 2004. Aeroflex Metelics. 24 Apr. 2006 <http://www.aeroflex-metelics.com/spiceStepRecovery.htm>.

[9] Stauffer, George H. "*SPICE Up the Development of a Step Recovery Diode Frequency Multiplier.*" June 1999. Dept. of Electrical Engineering, Capitol College, MD. 24 Apr. 2006 <http://www.ece.jhu.edu/∼pps/ECE777/ADMAT/CircDev/Pulse-GENERATORS-SHAPERS/freq-mult-SRD.pdf>